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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,958	10/30/2003	Kalyana Chakravarthy	852463.405	7801

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EXAMINER	
HASSAN, AURANGZEB	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,958	CHAKRAVARTHY ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 18 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5, 18 and 19 recites the limitation "the multiplexer" in lines 13, 9 and 2 respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 thru 9, 12, 13 and 18 thru 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Rust et al. (US Patent 5,699,530 hereinafter "Rust").

5. Referring to a buffer of claim 1, method of claim 5, and method of 18 Rust teaches buffers and methods comprising:

FIFO means capable of storing 'n' data words, each 'm' bits wide, having an 'm' bit wide data input terminal (column 1, lines 26 – 29);

Read data selection means (the data selector is represented by functionality of 102 and 104 with 110 having multiple outputs, where Read Pointer Matrix 110 is the selection means with multiple selection inputs, column 4, lines 30 - 33) connected to data output terminals of the FIFO (not shown in figure is the output precharge element inputted to the even and odd arrays, column 4, lines 54 – 50) means and having two data output terminals (two output terminals 112 and 114 of the even and odd arrays) providing simultaneous access to a selected storage location (column 4, lines 38 – 41);

Odd read pointer-generating (element 106, write pointer) means for providing the selection input to the data selection means for selecting data at an odd read address (element 104, column 4 lines 24 – 30);

Even read pointer-generating (element 106, write pointer) means for providing the selection input to the data selection means for selecting data at an even read address (element 102, column 4 lines 24 – 30);

Multiplexing means coupled to each of the two data output terminals (elements 112 and 114) of the read data selections means for selecting one of the outputs of the read data selection means as the first output of the FIFO (column 4, lines 34 – 41); and

State controlling means (signal 108 coupled to 118 via 120) coupled to the multiplexing means for controlling the selection of the final FIFO output and to the odd and even read pointer-generating means (column 4, lines 41 – 67).

6. Referring to a buffer of claim 2 and method of claim 6, Rust teaches buffers and methods comprising, FIFO status providing means coupled to a selected read pointer means for generating FIFO status signals (signals from elements 122 and 124, column 4, lines 49 – 53).

7. Referring to a buffer of claim 3, method of claim 7, and method of claim 20 Rust teaches buffers and methods comprising adder means coupled to the selected read pointer generating means to increment the read address for generating the next read address (column 1, lines 34 – 37).

8. Referring to a buffer of claim 4, method of claim 8, and method of claim 19 Rust teaches a buffer and methods wherein, said state controlling means can have two states namely, odd and even (column 2, lines 36 – 44).

9. Referring to a buffer of claim 9, Rust teaches a buffer, comprising,

a FIFO circuit configured to receive, store and output data (column 2, lines 53 – 62, read, store, write);

a data select circuit (the data selector is represented by functionality of 102 and 104 with 110 having multiple outputs, where Read Pointer Matrix 110 is the selection means with multiple selection inputs, column 4, lines 30 - 33) coupled to the FIFO circuit to receive and data from the FIFO circuit and having the first data output for outputting

even data and a second out for outputting odd data (elements 102 and 104, column 4 lines 24 – 30);

a multiplexer circuit (element 118) coupled to the first and second data outputs of the data select circuit and having a control input and a read data output (elements 112 and 114);

a finite station machine (state machine 34, figure 3) having an output coupled (via read pointer matrix, column 2, lines 10 – 22) to the control input of the multiplexer circuit, the finite state machine configured to generate a control signal to control the output of the multiplexer circuit (column 4, lines 34 – 41); and

a pointer circuit (figure 8) coupled to a further output of the finite state machine and configured to generate a read address that is the output to the data select circuit in response to a further control signal from the finite state machine (column 7 lines 9 – 14).

10. Referring to a buffer of claim 12 Rust teaches a buffer wherein, said state maintaining means can have two states namely, odd and even (column 2, lines 36 – 44).

11. Referring to a buffer of claim 13, Rust teaches a buffer wherein, the pointer circuit comprises an odd read pointer circuit and an even read pointer circuit, each coupled to the data select circuit and configured to select an odd read address and an even read address, respectively (elements 102 and 104, column 4 lines 24 – 30).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 10, 11, and 14 thru 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rust, in view of Kim et al. (US Pub No. 2002/0199042 hereinafter "Kim").

14. As per claims 14 and 17 Rust teaches a circuit comprising: a FIFO circuit configured to, receive, store and output (column 2, lines 53 – 62, read, store, write) words to a plurality of outputs, and control means coupled to the FIFO circuit comprising a data select circuit connected to the plurality of FIFO outputs (the data selector is represented by functionality of 102 and 104 with 110 having multiple outputs, where Read Pointer Matrix 110 is the selection means with multiple selection inputs, column 4, lines 30 - 33), the data select circuit having first and second data output buses (elements 112 and 114, precharged);

however Rust fails to explicitly teach a FIFO circuit configured to fetch a next word from the FIFO and assign it to one of the first and second data output buses that are not currently in use.

Kim teaches fetching and assigning following words from the FIFO and arranging for data output not in use (paragraph [0010 and 0011]). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Rust with the above teachings of Kim. One of ordinary skill in the art would have been motivated to make such modification in the processing of FIFO data output assignments.

15. Referring to a circuit of claim 15 Rust in view of Kim teaches a buffer wherein, the control means comprise a finite state machine (through element 18) coupled to a multiplexer (multiplexers 12 and 14) that is coupled to the data select circuit, the multiplexer having the first data output and the second data output as inputs and a read data output as an output (paragraph [0012]).

16. Referring to a buffer of claim 16 Rust in view of Kim teaches a buffer wherein; the finite state machine comprises a D-flip-flop (page 1, paragraph [0010] lines 13 – 15).

17. Referring to a method of claim 21, Rust teaches a method comprising using a data select circuit coupled to an output of the FIFO circuit and a multiplexer coupled to the multiple outputs of the data select circuit to assign the next word from the FIFO (figure 4 represents the data select in the form of even and odd arrays precharged by the outputs of the FIFO circuit and coupled to a multiplexer, the next word assigned by the pointer increment, column 5, lines 6 – 13).

18. Referring to a method of claim 22, Rust teaches a method comprising using a finite state machine to control a state of the multiplexer and a state of the data select circuit (state machine 34, figure 3).

Response to Arguments

19. Applicant's arguments filed 5/25/2006 have been fully considered but they are not persuasive. The applicant argues:

1) Rust does not show read data selector/selection means and state controlling means.

2) Rust does not show read data selector/selection means having two data output terminals providing simultaneous access to a selected storage location.

3) Rust does not show a finite state machine coupled to the multiplexer and to the odd and even read pointer-generating circuits.

4) Rust does not show fetching a next word from a FIFO circuit and assigning it to one of a first data out bus and a second out bus that is not currently in use.

20. In order assist the applicant to better understand the current rejection the Examiner has provided additional citations from Rust.

21. As per argument 1, the Examiner disagrees. The data selector is represented by functionality of 102 and 104 with 110 having multiple outputs, where Read Pointer

Matrix 110 is the selection means with multiple selection inputs, column 4, lines 30 – 33 with the state controlling means through signal 108 coupled to 118 via 120. Clearly from this citation, one of ordinary skill in the art would recognize the data selector/selection means illustrated by Rust.

22. As per argument 2, the Examiner disagrees. The data selector/selection means has two output terminals even 112 and odd 114 arrays figure 4 routed to a multiplexer 118 for simultaneous access to a selected storage location via the selection means 108 to 118 via 120 stated in above arguments response. Clearly from this citation one of ordinary skill in the art would recognize the two data output terminals providing simultaneous access to a selected storage location.

23. As per argument 3, the Examiner disagrees. Rust teaches a finite station machine 34, figure 3 having an output coupled via read pointer matrix, column 2, lines 10 – 22 to the control input of the multiplexer circuit, the finite state machine configured to generate a control signal to control the output of the multiplexer circuit column 4, lines 34 – 41. Clearly from this citation one of ordinary skill in the art would recognize the coupling of the finite state machine to the multiplexer via read pointer and even and odd arrays.

24. As per argument 4, the Examiner disagrees. Rust teaches a precharged, figure 7, to fetch the next word from a FIFO circuit and assigning it to one of a first data out

bus and second data out bus inputted into the even and odd arrays column 4, lines 54 – 66. The precharge element will appropriate fetch for the data out bus not in use as seen in column 5, lines 33 – 40. Clearly from this citation one of ordinary skill in the art would recognize fetching and precharging a first and second data out bus not in use.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Number 5,416,749 discloses an odd and even bank of registers comprised in a FIFO based data selection scheme as taught by the current application. Analogously a multiplexer is used to determine the choice of odd or even. The state thereon which the mux is chosen is by a flip-flop of subsequent state capabilities.

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER
8/21/06